What is claimed is:

1. A substrate comprising:

a gate pattern formed on a pixel region and a peripheral region, the pixel region and the peripheral region being disposed on the substrate;

an active pattern insulated from the gate pattern to be formed on the gate pattern, the active pattern including a semiconductor layer;

a data pattern electrically connected to a portion of the active pattern, said data pattern including a data electrode;

a first insulating interlayer formed on the data pattern, the first insulating interlayer having a first contact hole for partially exposing the data electrode of the data pattern, a second contact hole for exposing a gate electrode of a first drive transistor of the peripheral region, and a third contact hole for exposing a data electrode of a second drive transistor of the peripheral region; and

an electrode pattern part formed on the first insulating interlayer, the electrode pattern part including a first electrode pattern in contact with a data electrode of the pixel region through the first contact hole, and a second electrode pattern connecting the partially exposed gate electrode of the first drive transistor with the exposed data electrode of the second drive transistor through the second and third contact holes.

2. The substrate of claim 1, wherein the gate pattern includes a gate line and a gate electrode, the gate line is formed on the pixel region and the peripheral region, respectively, the gate electrode is branched from the gate line, and the substrate further comprises a lower capacitor electrode formed on the pixel region of the substrate, the first lower capacitor electrode being made from a same layer as the gate line, the lower

capacitor electrode being spaced apart by a selected interval from the gate line and being in parallel with the gate line.

3. The substrate of claim 1, wherein the gate pattern includes a gate line and a gate electrode, the gate line is formed on the pixel region and the peripheral region, respectively, the gate electrode is branched from the gate line, and the substrate further comprises a lower capacitor electrode formed on a gate driving region of the peripheral region of the substrate, said lower capacitor electrode being made from the same layer as the gate line and extending from one side edge of the gate line, the peripheral region comprising the gate driving region and a pad region.

4. The substrate of claim 1, wherein the active pattern is comprised of amorphous silicon.

5. The substrate of claim 1, wherein the peripheral region has a gate driving region and a pad region, the data electrode includes a first electrode or a second electrode, and the first and second electrode of the first and second drive transistors has an interdigital structure.

6. The substrate of claim 5, wherein the second electrode of the second drive transistor has an upper capacitor electrode extending toward the first electrode of the first drive transistor.

7. The substrate of claim 1, wherein the first insulating interlayer is comprised of silicon nitride.

8. The substrate of claim 1, wherein the first insulating interlayer is comprised of a photosensitive organic insulating material.

9. The substrate of claim 8, wherein the first insulating interlayer has an embossing formed on a surface of the first insulating interlayer.

10. The substrate of claim 1, wherein the first, second and third electrode patterns are comprised of a transparent material.

11. The substrate of claim 10, wherein the transparent material includes indium tin oxide (ITO) or indium zinc oxide (IZO).

12. The substrate of claim 1, wherein the active pattern and the data electrode have first and second end surfaces, respectively, and each of the first and second end surfaces has substantially the same slope each other.

13. A substrate comprising:

a gate pattern formed on a pixel region and a peripheral region, the pixel region and the peripheral region being disposed on the substrate;

an active pattern insulated from the gate pattern to be formed on the gate pattern;

a data pattern electrically connected to a portion of the active pattern, said data pattern including a first electrode, a second electrode and a data line coupled to the first electrode;

a first insulating interlayer formed on the data pattern, the first insulating interlayer including a first contact hole for partially exposing the second electrode, a second contact hole for partially exposing the first electrode of the pixel region, a third contact hole for exposing a gate electrode of a first drive transistor of the peripheral region, and a fourth contact hole for exposing a data electrode of a second drive transistor of the peripheral region; and

an electrode pattern part formed on the first insulating interlayer, the electrode pattern part including a first electrode pattern coupled to a second electrode of the pixel region through the first contact hole, a second electrode pattern coupled to a first electrode of the pixel region through the second contact hole, and a third electrode pattern connecting the exposed gate electrode of the first drive transistor with the exposed data electrode of the second drive transistor through the third and fourth contact holes.

14. The substrate of claim 13, wherein the gate pattern includes a gate line and a gate electrode, the gate line is formed on the pixel region and the peripheral region, respectively, the gate electrode is branched from the gate line, and the substrate further comprises a lower capacitor electrode formed on the pixel region of the substrate, said lower capacitor electrode being made from a same layer as the gate line, and the lower capacitor electrode being spaced apart by a selected interval from the gate line and being in parallel with the gate line.

15. The substrate of claim 13, wherein the gate pattern includes a gate line and a gate electrode, the gate line is formed on the pixel region and the peripheral region, respectively, the gate electrode is branched from the gate line, and the substrate further

comprises a lower capacitor electrode formed on a gate driving region of the peripheral region of the substrate, said lower capacitor electrode being made from a same layer as the gate line and extending from one side edge of the gate line, the peripheral region having the gate driving region and a pad region.

16. The substrate of claim 13, wherein the active pattern is comprised of amorphous silicon.

17. The substrate of claim 13, wherein the peripheral region includes a gate driving region and a pad region, and the first and second electrodes of the first and second drive transistors have an interdigital structure.

18. The substrate of claim 17, wherein the second electrode of the second drive transistor has an upper capacitor electrode extending toward the first electrode of the first drive transistor.

19. The substrate of claim 13, wherein the first insulating interlayer is comprised of silicon nitride.

20. The substrate of claim 13, wherein the first insulating interlayer is comprised of a photosensitive organic insulating material.

21. The substrate of claim 20, wherein the insulating interlayer has an embossing formed on a surface of the insulating interlayer.

22. The substrate of claim 13, wherein all the first, second and third electrode patterns are comprised of a same material.

23. A method for manufacturing a substrate, comprising:

forming a gate pattern on a pixel region and a peripheral region of the substrate;

forming a gate insulating film on the substrate having the gate pattern;

forming an active pattern on the gate insulating film, the active pattern including a semiconductor layer;

forming a data pattern including a first electrode, a secondelectrode , and a data line coupled to the second electrode;

forming an insulating interlayer on the data pattern;

forming a first contact hole for partially exposing a first electrode of the pixel region, a second contact hole for exposing a gate electrode of a first drive transistor of the peripheral region and a third contact hole for exposing a data electrode of a second drive transistor of the peripheral region by partially etching the insulating interlayer;

forming a conductive film on the insulating interlayer having the first, second, and third contact holes; and

forming a first electrode pattern and a second electrode pattern by patterning the conductive film, the first electrode pattern being coupled to the first electrode of the pixel region through the first contact hole and the second electrode pattern connecting the exposed gate electrode of the first drive transistor with the exposed data electrode of the second drive transistor through the second and third contact holes.

24. The method of claim 23, wherein the gate pattern includes a gate line and a gate electrode, the gate line is formed on the pixel region and the peripheral region,

respectively, the gate electrode is branched from the gate line, , said gate pattern being made from a same layer as the gate line, and further including a first lower capacitor electrode which is spaced apart by a predetermined interval from the gate line and is in parallel with the gate line and a second lower capacitor electrode which is formed on the peripheral region of the transparent insulating substrate and is extending from one side of the gate line.

25. The method of claim 23, wherein the peripheral region comprises a gate driving region and a pad region, and the data pattern of the gate drive region comprises the second and first electrodes of the first and second drive transistors, the second and first electrodes having an interdigital structure.

26. The method of claim 25, wherein the first electrode of the first drive transistor of the gate driving region has an upper capacitor electrode extending toward the second electrode of the second drive transistor.

27. The method of claim 23, wherein the active pattern is comprised of amorphous silicon.

28. A method for manufacturing a substrate, comprising:

forming a gate pattern on a pixel region and a peripheral region of the substrate;

forming a gate insulating film on the substrate having the gate pattern;

forming an active pattern on the gate insulating film, the active pattern including a semiconductor layer;

forming a data pattern including a first electrode, a second electrode and a data

line coupled to the source electrode;

forming an insulating interlayer on the data pattern and the gate insulating film;

forming a first contact hole for partially exposing the second electrode of the pixel region, a second contact hole for partially exposing the first electrode of the pixel region, a third contact hole for exposing a gate electrode of a first transistor of the peripheral region and a fourth contact hole for exposing a data electrode of a second transistor of the peripheral region by partially etching the insulating interlayer;

forming a conductive film on the first insulating layer having the first, second, third, and fourth contact holes; and

forming a first electrode pattern, a second electrode pattern, and a third electrode pattern by patterning the conductive film, the first electrode pattern being coupled to a second electrode of the pixel region through the first contact hole, the second electrode pattern being coupled to a first electrode of the pixel region through the second contact hole and the third electrode pattern connecting the exposed gate electrode of the first transistor with the exposed data electrode of the second transistor through the third and fourth contact holes.

29. The method of claim 28, wherein the gate pattern includes a gate line and a gate electrode, the gate line is formed on the pixel region and the peripheral region, respectively, the gate electrode is branched from the gate line, the gate pattern is made from a same layer as the gate line, and comprises a first lower capacitor electrode spaced apart by a predetermined interval from the gate line and parallel to the gate line and a second lower capacitor electrode formed on the peripheral region of the substrate and from the same layer as the gate line and extending from one side of the gate line.

30. The method of claim 28, wherein the peripheral region comprises a gate driving region and a pad region, and the data pattern of the gate drive region comprises the second and first electrodes of the first and second drive transistors, the second and first electrodes having an interdigital structure.

31. substrate comprising:

a gate pattern formed on a pixel region and a peripheral region, the pixel region and the peripheral region being disposed on the substrate;

an active pattern insulated from the gate pattern to be formed on the gate pattern, the active pattern including a semiconductor layer;

a data pattern electrically connected to a portion of the active pattern; and

a first insulating interlayer formed on the data pattern, wherein the pixel region includes a plurality of pixels and the active pattern is comprised of amorphous silicon.

32. The substrate of claim 31, wherein the pixels respectively includes a first transistor, and the peripheral regions includes a plurality of driver transistors for driving the first transistor of the pixels.

33. The substrate of claim 31, wherein the data pattern includes a data electrode, the first insulating interlayer has a first contact hole for partially exposing the data electrode of the data pattern, a second contact hole for exposing a gate electrode of a first drive transistor of the peripheral region, and a third contact hole for exposing a data electrode of a second drive transistor of the peripheral region, and the substrate further includes an electrode pattern part formed on the first insulating interlayer, the electrode pattern part including a first electrode pattern in contact with a data electrode

of the pixel region through the first contact hole, and a second electrode pattern connecting the partially exposed gate electrode of the first drive transistor with the exposed data electrode of the second drive transistor through the second and third contact holes.

34. The substrate of claim 31, wherein the first, second and third electrode patterns are comprised of a transparent material.

35. The substrate of claim 34, wherein the transparent material includes indium tin oxide (ITO) or indium zinc oxide (IZO).